Simulation of unified architecture of IEEE 802.11a and 802.16a PHY layers using MATLAB

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Abstract— WiFi and WiMAX are widely used wireless technologies for accessing internet. This paper elaborates the simulation of unified architecture physical layers of WiFi and WiMAX technologies which are compliant to IEEE standards 802.11a and 802.16a respectively. The PHY specifications of these standards are described with block schematics. SIMULINK based simulation of the block schematics of these two technologies is done and the results of packet error rate are studied as compared to the data rates specified in the standards. A comparative analysis is done based on the OFDM parameters and their variations in the two technologies. The scope of this paper is limited to the digital signal processing involved in the PHY layers of WiFi and WIMAX technologies.

Keywords: OFDM, WiFi, WiMAX, SIMULINK

1. Introduction

WiFi and WiMAX are the well developed and standardized technologies working on OFDM platform. Their physical layer architecture are much similar accept WiMAX physical layer has RS encoder & Decoder at transmitter and receiver respectively. In this paper the physical layer specification similarities and differences of IEEE 802.11a (WiFi) and IEEE 802.16a (WiMAX) are discussed. We used the conventions for WiFi as 11a and WiMAX as 16a for the entire paper.The architecture of PHY layer of the IEEE 802.16a is similar to IEEE 802.11a except some differences are stated as below.

Table 1. Architectural differences between IEEE 802.11a and IEEE 802.16a

| Parameters	IEEE 802.11a	IEEE 802.16a
Scrambler	7 bits	15 bits
FEC coder (Reed Solomon) encoder profile (N,K,T) supported	Not present	(255,239,8) (12,12,0), (32,24,4), (40,36,2), (64,48,8), (80,72,4), (108,96,6), (120,108,6)
FEC coder (Convolutional coder) Code rates	1/2, 2/3 , 3/4	1/2, 2/3, 3/4, 5/6
Interleaver Block Size	48, 96, 192, 288	192, 384, 768, 1152
Pilot/Guard Insertion Pilot indices Guard indices	-21, -7, 7, 21 -32 to -27, 0, 27 to 31	-88, -63, -38, -13, 13, 38, 63, 88 -128 to -101, 0, 101 to 127
IFFT Size	64	256
CP insertion CP size Short Preamble Long Preamble	16 (32 for preamble) 8 16-sample symbols 2 64-sample symbols	8, 16, 32, 64 4 64-sample symbols 2 128-sample symbols
S/P symbol / CP sizes	64 / 16	256 / 8, 16, 32, 64
FFT Size	64	256
Deinterleaver Block Size	48,96,192,288	192, 384, 768, 1152
Reed Solomon Decoder Reed Solomon Settings	Not present	Same as Reed Solomon Encoder
Descrambler LFSR settings	Same as Scrambler	Same as Scrambler

The organization of paper is as follows. Section 1 contains the comparison of physical layers of 11a and 16a. Section 2 contains the description of block diagrams of SIMULINK model for unified architecture of 11a and 16a. We conclude in section 3.

2. SIMULINK based simulation of unified architecture of 802.11a and 802.16a PHY layers
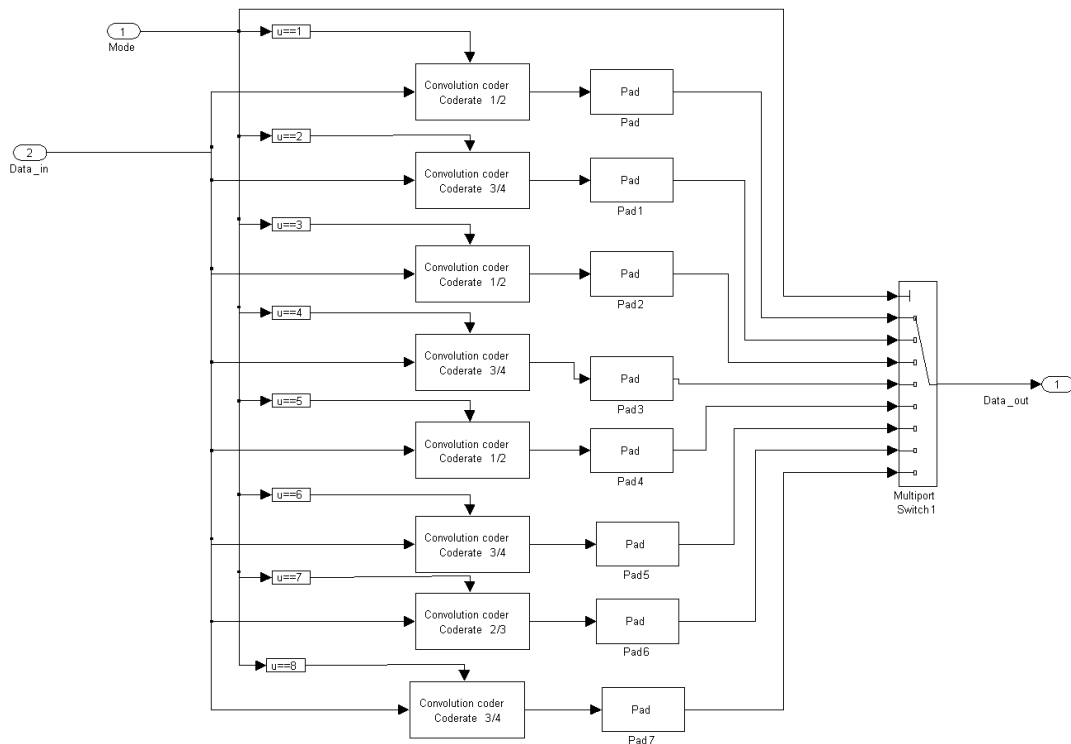
Description of each block of the SIMULINK system and their respective hierarchy levels are described below. Each block is shown by its hierarchy level that denotes the level at which the block is placed in the system. Hierarchy level 0 is Top level containing the top parent blocks. The first level subsystem blocks are shown as Hierarchy level 1. The level 2 subsystems are the child blocks of Hierarchy level 1.

1) Variable data rate block:
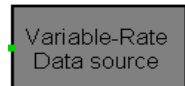
Figure 1. Variable rate data source(Hierarchy level 0)

- Generates random data input: 6,9,12,18,24,36,48,54 Mbps for

different code rates. This block performs Forward error correction operation on input data stream.
The internal blocks of this block are shown as below.

- As per the specification of 802.11a and 16a the convolutional encoder used works on code rates of 1 / 2 , 3 / 4, 2/3, 5/6(for 16a).
- The multiport switch block chooses between a number of inputs.
- The pads are used to match dimensions of the output of CC coder on every pins of the multi port switch.

Figure 3. Internal blocks of Convolution Encoder Bank (Hierarchy level 1)

11a and 12,18,24,36,48,72,96,108 Mbps for 16a configuration.
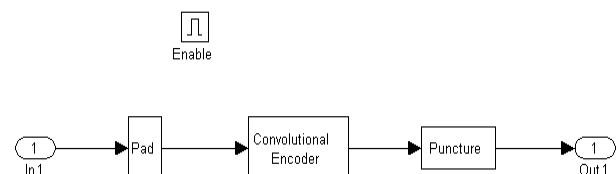
2) Convolutional Encoder Bank:
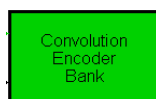
Figure 2. Convolution Encoder Bank(Hierarchy level 0)

- Contains CC coder blocks with

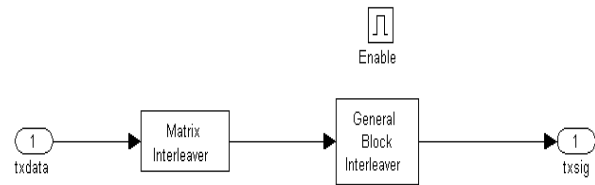**Figure 4.** Internal blocks of Convolutional encoder(Hierarchy level 2)

- The convolutioal encoder

performs the encoding operation. The puncture block selects a particular code rate.
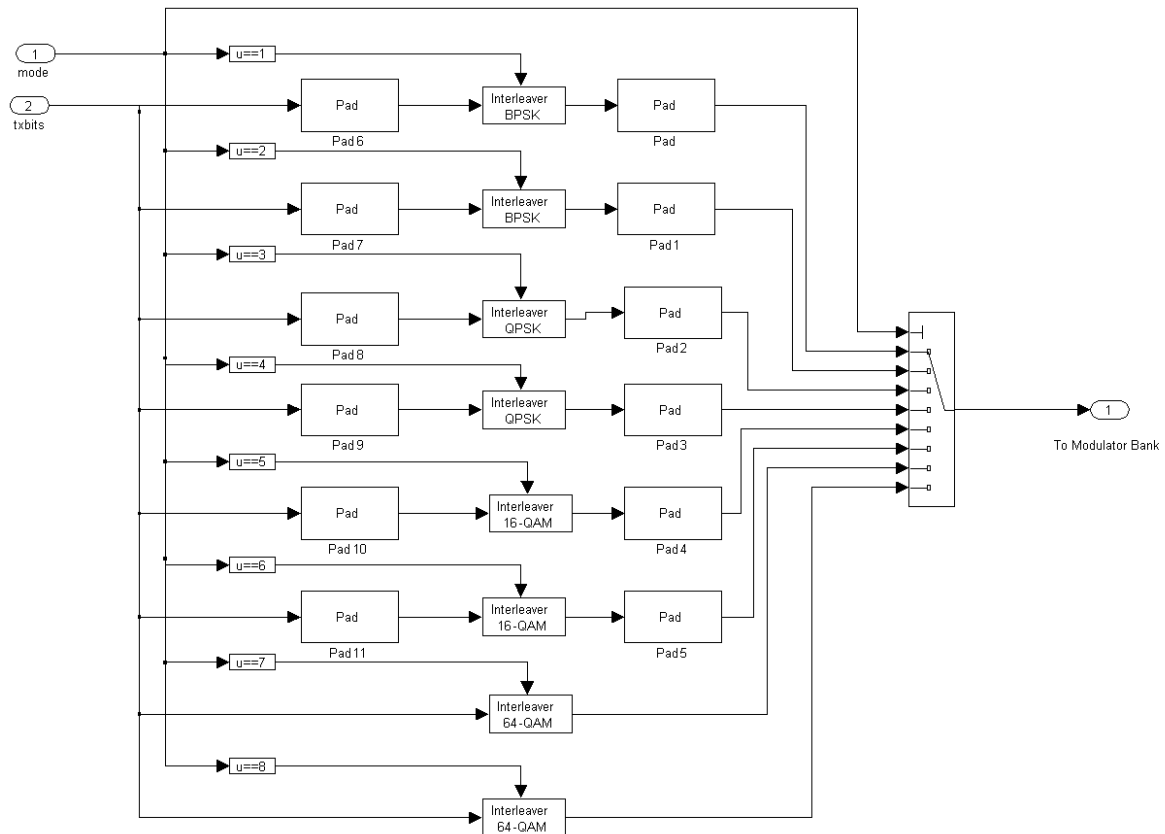
3) Interleaver Bank:

Figure 5. Interleaver Bank(Hierarchy level 0)

Figure 7. Internal blocks of interleaver(Hierarchy level 2)

- Inside the interleaver blocks two interleaver blocks are cascaded.

Figure 6. Internal blocks of Interleaver bank(Hierarchy level 1)

- This block performs interleaving operation on the encoded bit stream.

The internal blocks of this block are shown below.

- The pads are used for matching the dimensions of inputs of interleaver blocks.

- Matrix interleaver
- Block interleaver

4) Modulator bank:

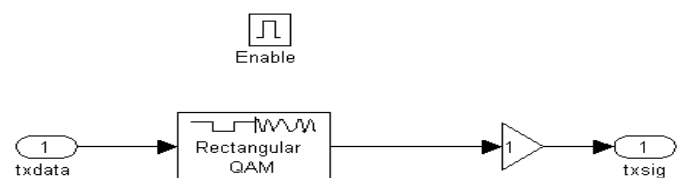**Figure 8.** Modulator Bank(Hierarchy level 0)
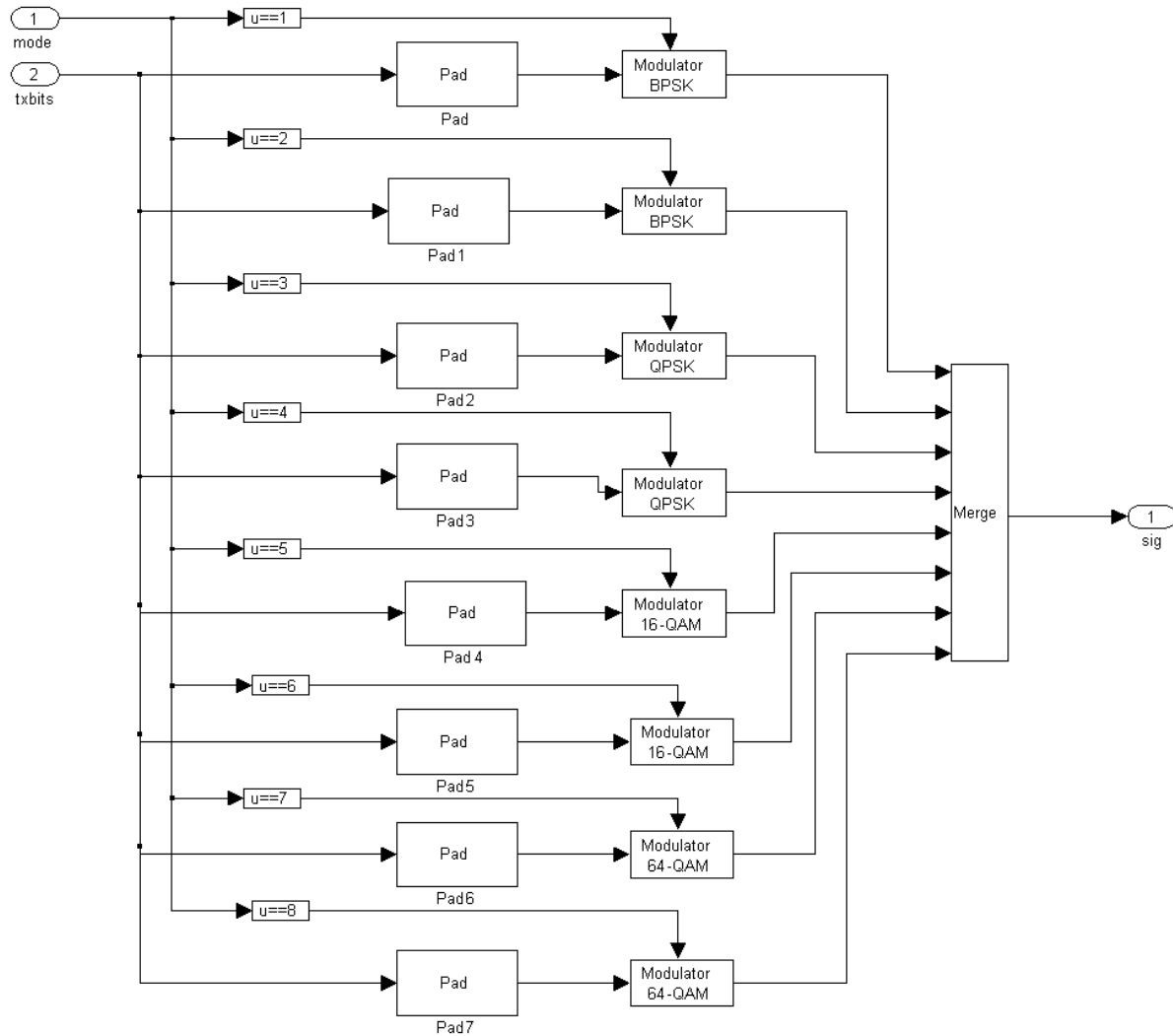
Figure 9. Internal Blocks of Modulator Bank(Hierarchy level 1)

- This block performs QAM modulation on the interleaved bit stream. It will output complex numbers assigned to a group of bits.

The internal blocks of this block are as shown below.

- Each modulator block is named as per the M-ary modulation performed by the modulator block. Depending on mode the m-ary number is changed from 2,4,16 and 64 referring to BPSK, QPSK, 16 QAM and 64-QAM. The mapping schemes for 11a and 16a are same.
- The Merge block combines its inputs into a single output line whose value at any time is equal to the most recently computed output of its driving blocks.

**Figure 10.** Internal Blocks of Modulator(Hierarchy level 2)

5) Serial to parallel block:
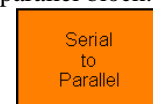
Figure 11. Serial to parallel converter block(Hierarchy level 0)

- This blocks is used to insert the pilot carriers and DC components to the bit stream and to convert the serial data into parallel data carriers which can be given as input to the IFFT block.
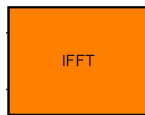
Internal block diagram of this block is as given below.
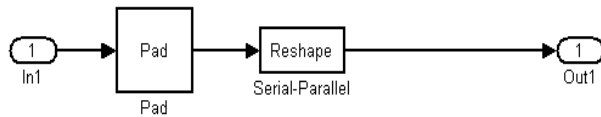
Figure 1 Internal blocks of serial to parallel converter block(Hierarchy level 1)

- The Reshape block changes the dimensionality of the input signal to a dimensionality that you specify, using the block's Output dimensionality parameter.
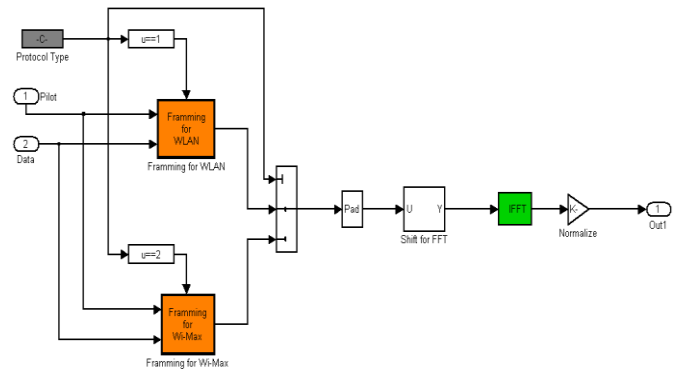
6) IFFT block:

Figure 2 IFFT block(Hierarchy level 0)

- The IFFT block computes the inverse fast Fourier transform (IFFT) of each channel of a P-by-N or length-P input, u. When the

Inherit FFT length from input dimensions check box is selected, the input length P must be an integer power of two, and the FFT length M is equal to P.

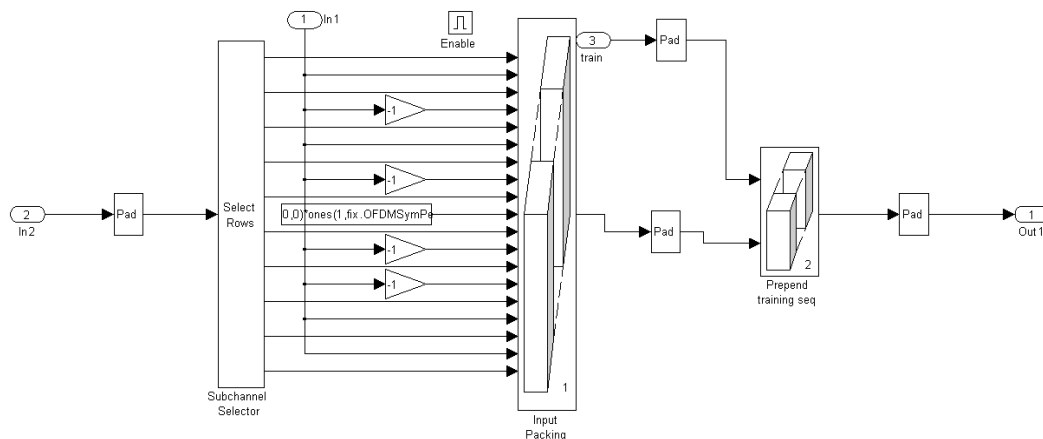The internal blocks of this block are as shown below

Figure 5 Internal blocks of IFFT blocks(Hierarchy level 1)

- Depending on the protocol type set in the system settings block the framing blocks are chosen. The pad provides the length of data compatible with IFFT.
- The IFFT points are inherited from the data
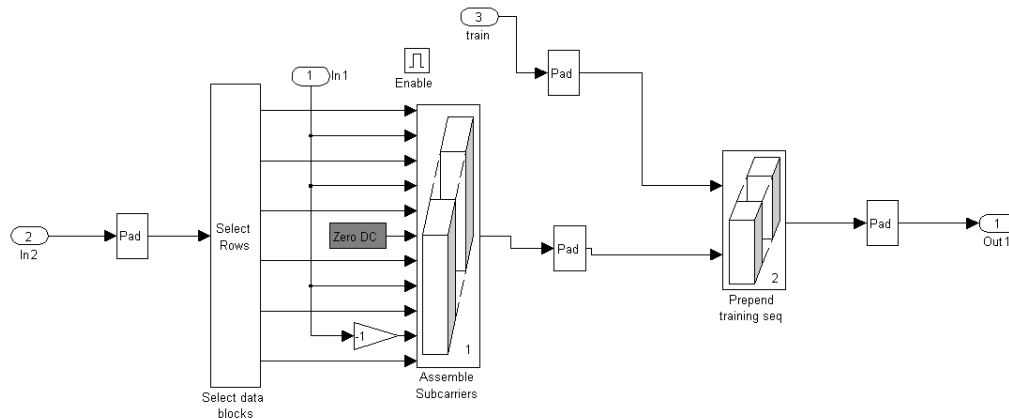
Figure 3 Internal blocks of Framing for WLAN(Hierarchy level 2)

Figure 4 Internal blocks of Frammig for 16a(Hierarchy level 2)

dimensions. The framming blocks make the data dimension 64 and 256 for 11a and 16a respectively.

- The select rows block selects the inputs of concatenate block(Assemble subcarrier). The concatenate block combines the data carriers, pilot carriers and training carriers.

- The Framing blocks are used to make the parallel bit stream to be compatible with the Inputs of the IFFT block. The Pad adds extra zero bits to the input pins of IFFT to assure same length of data at each pins of IFFT.
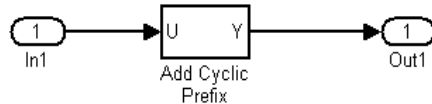
7) Cyclic prefix insertion block:

Figure 6 Cyclic prefix block(Hierarchy level 0)

- This block adds the portion of input frame to its front end. Thus inserting a guard interval. For 11a 16 bits and for 16a 64 bits are the CP lengths.

The internal block of cyclic prefix is as shown in figure.

Figure 7 Internal block of Cyclic prefix block(Hierarchy level 1)
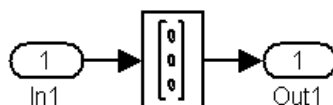
- Selector Block: The Selector block generates as output selected or reordered elements of an input vector, matrix, or multidimensional signal. A Selector block accepts vector, matrix, or multidimensional signals as input.

8) Parallel to serial block:

Figure 8 Parallel to serial block(Hierarchy level 0)

The internal block diagram of this block is as shown below.

Figure 9 Internal blocks of Parallel to serial block(Hierarchy level 1)

- The reshape function is used to convert the

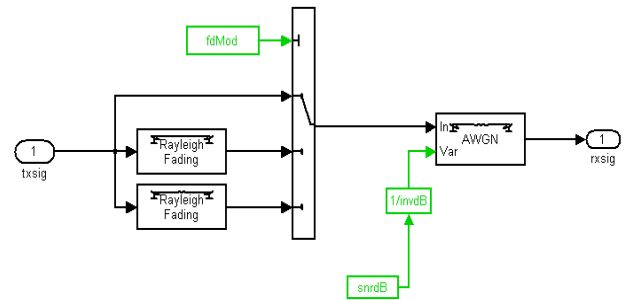parallel data streams to serial bit stream.

9) Wireless channel:

Figure 10 Wireless channel (Hierarchy level 0)

- The wireless channel is used to insert noise in the OFDM modulated data. There are three options
  - No noise
 - Non dispersive multipath noise
  - Dispersive multipath noise

The internal blocks of this block is shown as below

Figure 11 Internal blocks of Wireless channel(Hierarchy level 1)

- As shown in figure the multi port switch selects one of the three options stated above. After this the AWGN noise is added to the bit stream with user defined level of noise power (in dB).
  1) Multipath Rayleigh Fading channel
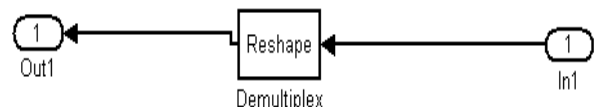 2) AWGN channel(Addative White Gaussian Noise)

10) Serial to parallel block at receiver:
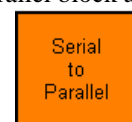
Figure 12 Serial to parallel block at receiver(Hierarchy level 0)

- This block performs inverse operation of parallel to serial block of transmitter.

The internal blocks are as shown below.

Figure 13 Internal blocks of serial to parallel block at receiver(Hierarchy level 1)

- Reshape is a library block that converts the dimension of a matrix to the input dimensions
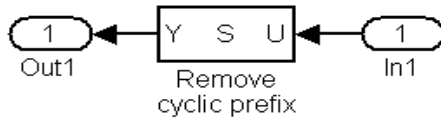
11) Remove cyclic prefix block:

Figure 14 Remove cyclic prefix block(Hierarchy level 0)

- This block removes the cyclic prefix part from the input bit stream.

The internal blocks of this block are as shown below.

Figure 15 Internal blocks of remove cyclic block(Hierarchy level 1)

- This block uses a selector block which will select only the desired part of the input bit stream and drop the cyclic prefix part.
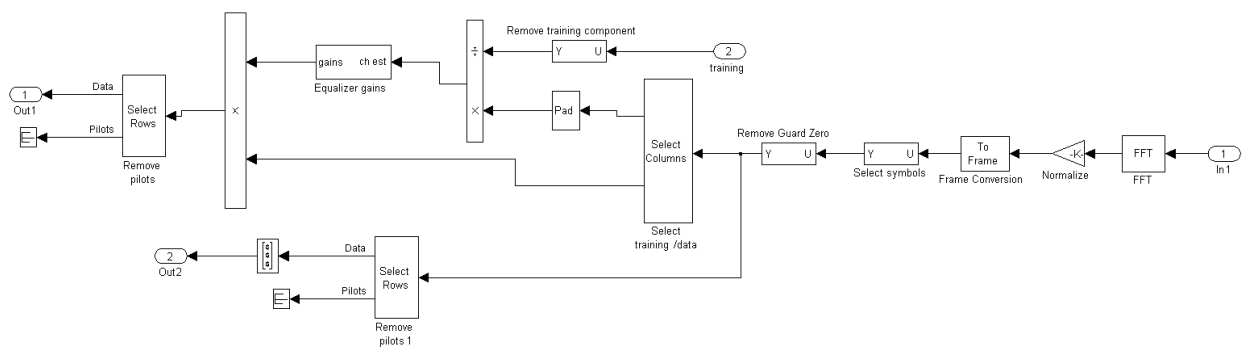
12) FFT block:

Figure 16 FFT block(Hierarchy level 0)

- This block performs the inverse operation of the IFFT block and will convert the time domain data to frequency domain.

The internal block diagram is as shown below.

- This block also removes the DC zeros contained in the input data. The pilots are extracted and discarded. The training sequence given is multiplied by the input

data. The result is given to equalizer gain block which performs the averaging operation and stabilizes the constellation. The data is further sent to the next block.
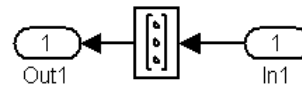
13) Disassemble OFDM frames:

Figure 29 Disassemble OFDM frames block(Hierarchy level 0)

- This block converts the parallel data carriers to serial carrier

The internal block diagram is as shown below.

Figure 10 Parallel to serial converter(Hierarchy level 1)

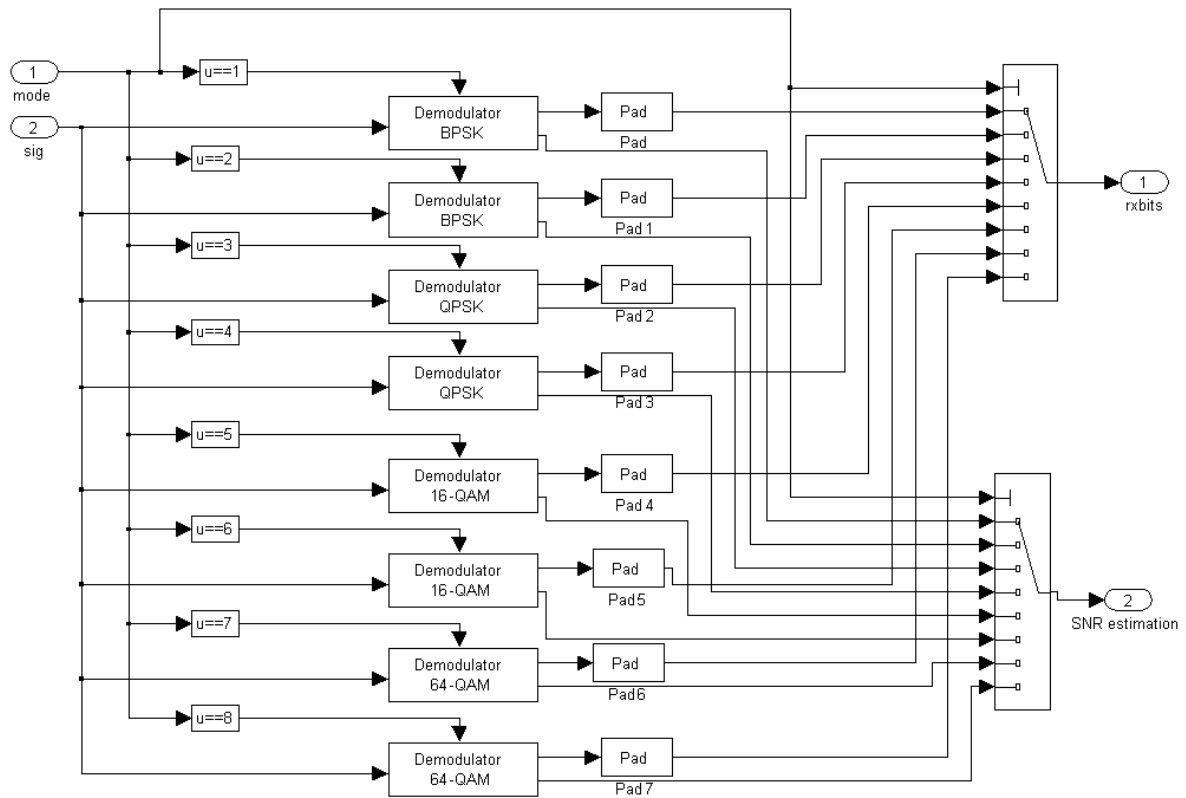- It performs the parallel to serial operation.
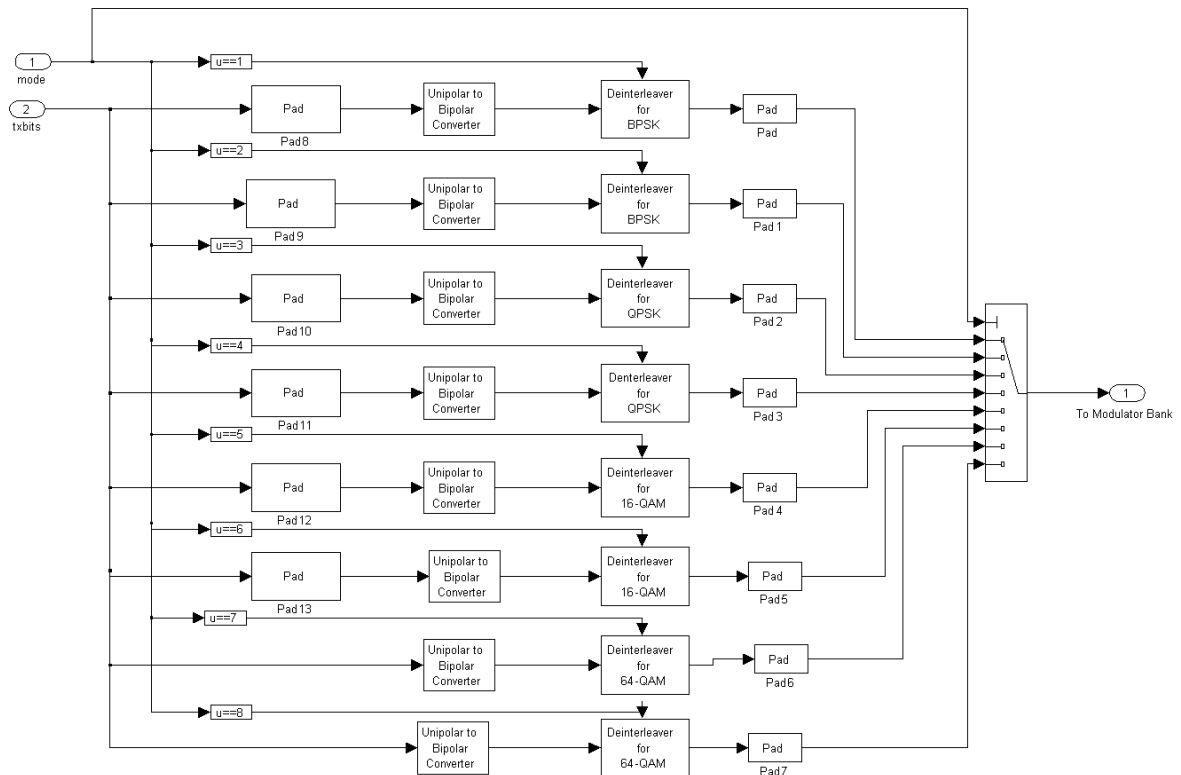
14) Demodulator Bank:

Figure 21 Demodulator Bank(Hierarchy level 0)

- The demodulator bank recovers digital bits from the modulation symbols.

The internal diagram of this block is as shown below

**Figure 28** Internal block diagram of FFT block(Hierarchy level 1)

Figure 42 Internal diagram of Demodulator bank(Hierarchy level 1)

Figure 35 Internal block diagram of Deinterleaver bank(Hierarchy level 1)

- As shown in figure 2.1.27, various demodulators such as BPSK, QPSk, 16-QAM and 64 QAM are used to demodulate the data. As per the mode the respective demodulator bank. The demodulator blocks are enabled sub systems which are controlled by the function blocks, u==1, u==2, etc. The Pads are used to equalise the output of Demodulator blocks. This is done because the multiport switch can not take different dimensions of data.
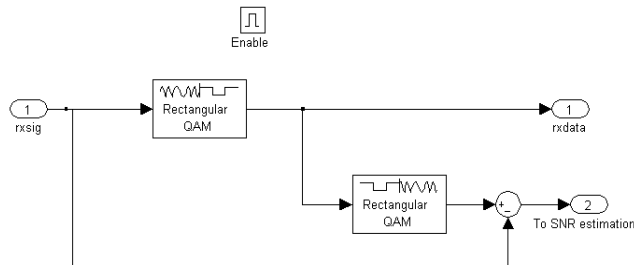
Figure 53 Internal blocks of Demodulator block(Hierarchy level 2)

- Here the demodulated data is given to deinterleaver bank as well as to SNR estimation block.
- The rectangular QAM block performs the demapping of data and recovers the original bitstream. The bitstream is again modulated and subtracted with the received data. This data is given to SNR estimation block.
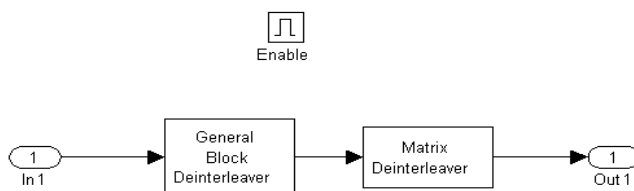
15) Deinterleaver Bank:

Figure 64 Deinterleaver Bank block(Hierarchy level 0)

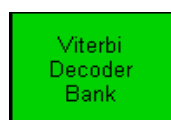- This block performs the deinterleaving operation on the demodulated data.

The internal block diagram is as shown below

Figure 36 Internal blocks of Deinterleaver(Hierarchy level 2)

- The general and matrix interleaver performs two permutation (rearranging) of data to get the encoded data.
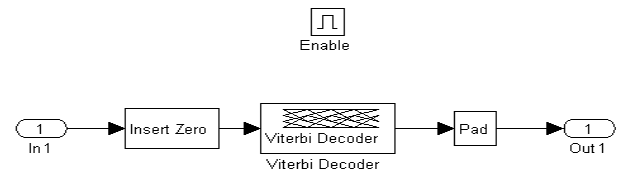
16) Viterbi decoder Bank:

Figure 37 Viterbi Decoder Bank block(Hierarchy level 0)

- This block recovers the original

information data inserted to by random data generator, by decoding the coded bitstream using viterbi decoder blocks.The internal block diagram is shown as below.

- As per the mode, respective viterbi decoder will be selected. The viterbi block estimates the correct data based on maximum likelihood algorithm. Various code rates are 1/2, 2/3, 3/4 and 5/6, where 5/6 is only used in 16a implementation. For code rates 2/3, 3/4 and 5/6 depuncturing is done before applying them to viterbi decoder block

Figure 39 Internal blocks of Viterbi decoder(Hierarchy level 2)

- The insert zero block performs the de-puncturing operation. The viterbi decoder block estimates the correct data using trellis diagram.
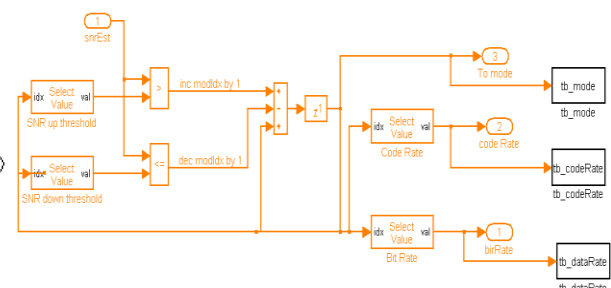
17) Mode Control:

**Figure 70** Mode Control(Hierarchy level 0)

- This block takes input from SNR estimation block and changes the mode of the system accordingly. When SNR is higher then mode will be increased towards 8 and when SNR is lower the mode is decreased towards 1.

The internal block diagram of this block is as shown below.

Figure 81 Internal blocks of Mode control block(Hierarchy level 1)

- The select value blocks select a value from snrup matrix and snrdn matrix.
- These matrices contains SNR values for which the data rates are supposed to changes.
- The comparison block gives incremented or decremented index value. This index value actually selects a matrix value from Mode, Code rate , data rate and snrup and snrdn
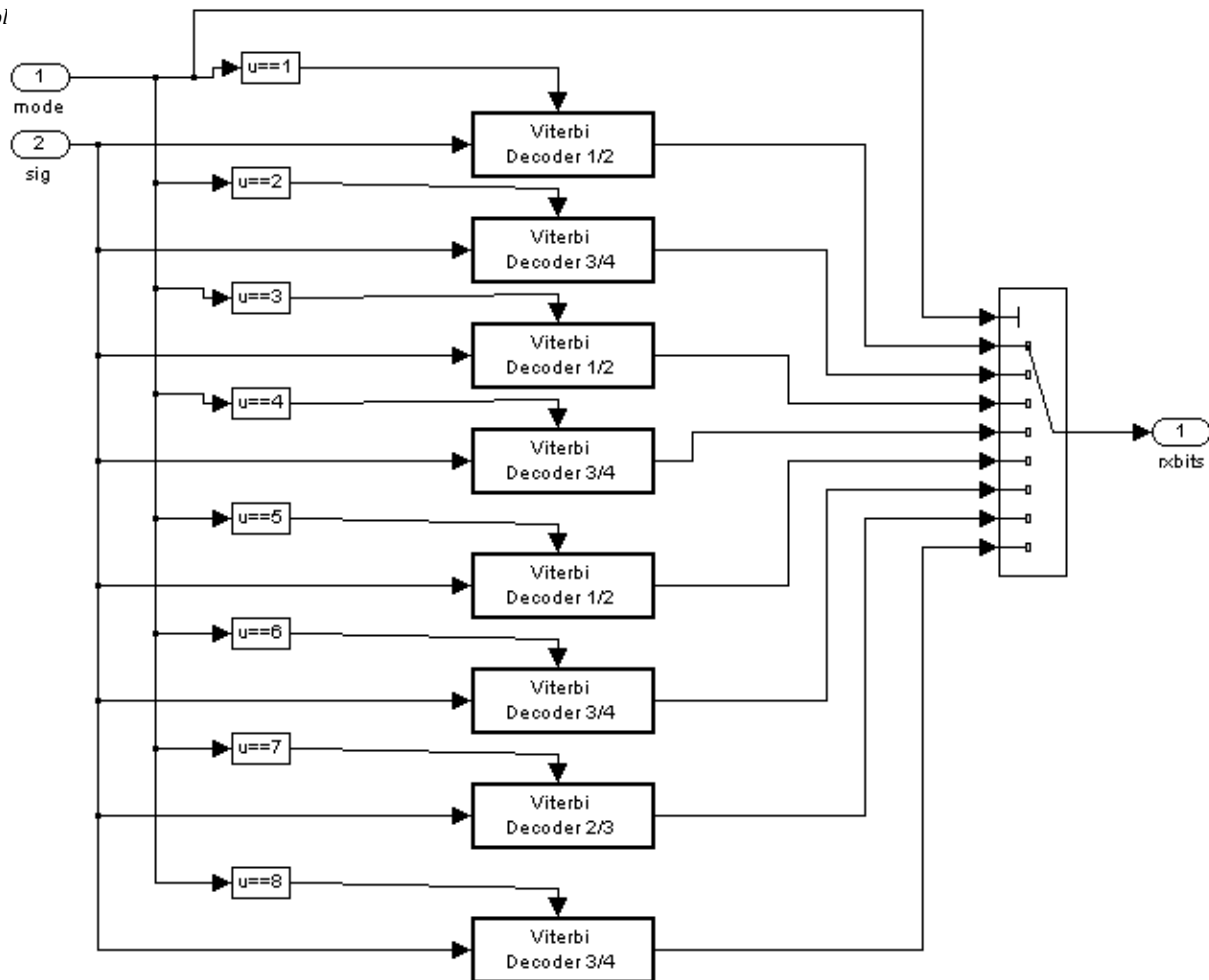
Figure 38 Internal blocks of Viterbi decoder Bank(Hierarchy level 1)

matrices.

- Mode output is used to configure Variable data rate source, Convolution encoder bank, Interleaver bank and Modulator bank at transmitter and to demodulator bank, deinterleaver bank and viterbi decoder bank at receiver.

- The tb_mode, tb_codeRate and tb_datarate are To workspace blocks used to export the simulation data to excel spreadsheet.

The example of simulation data porting to excel spreadsheet is as shown below.

Table 2 Simulation data poted to Excel worksheet

| Mode	Code_Rate	Data_Rate	Modulation_Scheme
6	0.75	36	16-QAM
5	0.5	24	16-QAM
4	0.75	18	QPSK
3	0.5	12	QPSK
2	0.75	9	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK
1	0.5	6	BPSK

1. SIMULINK model for IEEE 802.11a and 802.16a

Fig 2.1 shows the SIMULINK model compatible for 11a and 16a PHY layers. The System settings block configures the model in 11a or 16a with number of OFDM symbols to be processed at a time.
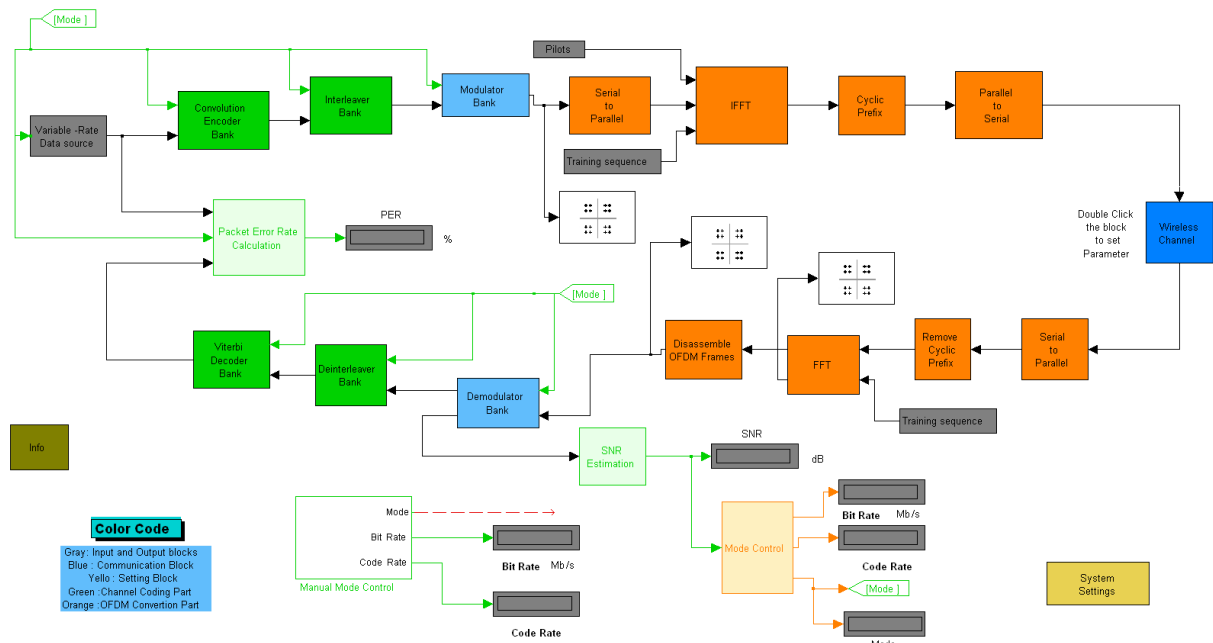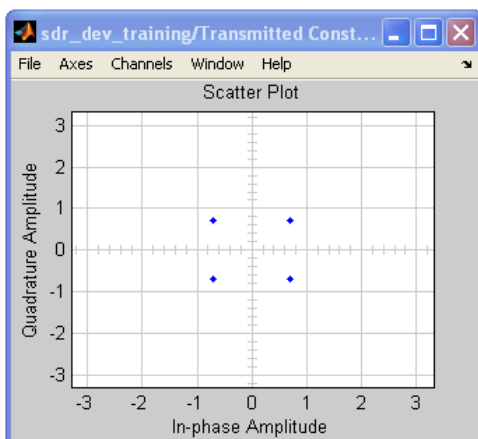
Figure 42. SIMULINK Schematic for Combined Configuration of 11a and 16a
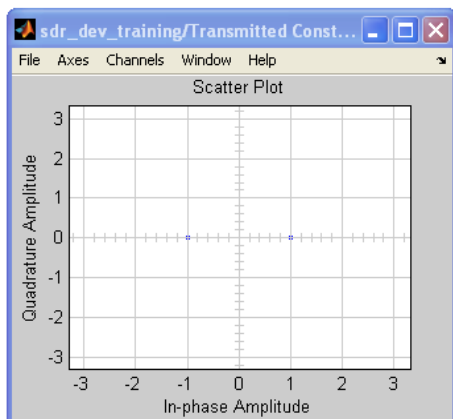
Figure 43(a). Transmitted Constellation
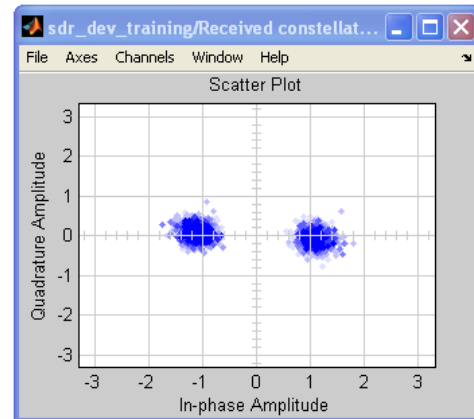
Figure 43(b). Received Constellation with equalization

Figure 44(a). Transmitted Constellation

Figure 44(b). Received Constellation with equalization

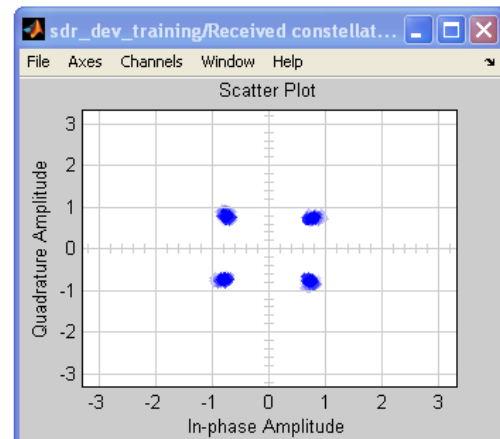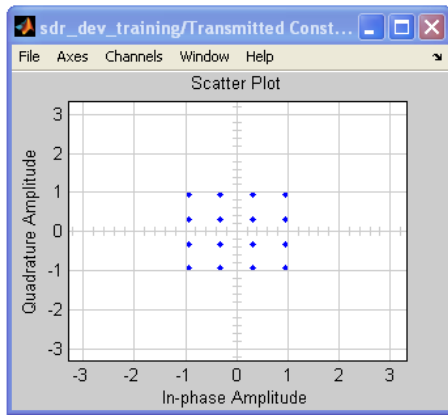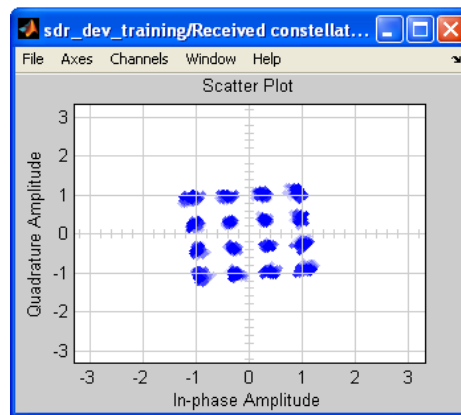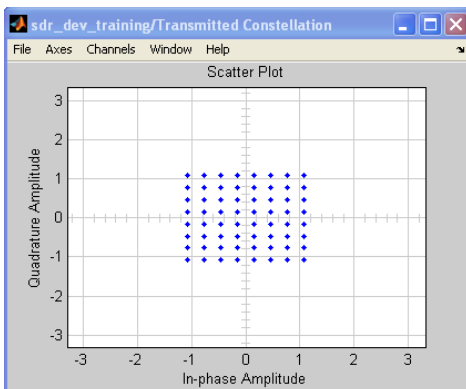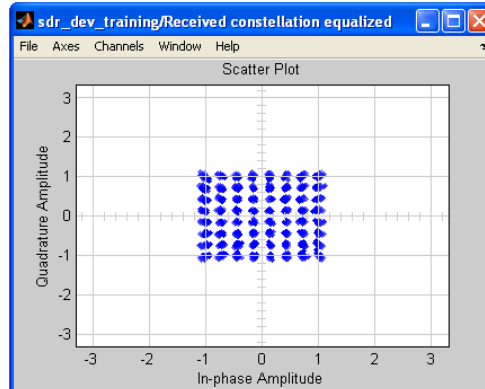The colors show the classification of the block in

Figure 45(a). Transmitted Constellation

Figure 45(b). Received Constellation with equalization

Figure 46(a). Transmitted Constellation

Figure 46(b). Received Constellation with equalization

Input and Output blocks, Communication blocks, setting blocks, Channel coding blocks and OFDM conversion block. Color codes for SIMULINK system are as follows

1) Gray : Input and output block
2) Blue: Communication block
3) Yellow: System setting block
4) Green: Channel coding block
5) Orange: OFDM Block

Above schematic is also supported by SDR_settings.m file which includes the initialization of the 11a and 16a blocks. Here the scrambler is not included for simulation purpose because the source itself is a random source and long strings of 0s and 1s are avoided.

Constellations Transmitted and received:

For BPSK (Data rate 6 and 9 for 11a and 12 and 18 for 16a) as shown in Figure 43(a, b)

For QPSK (Data rate 12 and 18 for 11a and 24 and 36 for 16a) as shown in Figure 44(a, b)

For 16-QAM (Data rate 12 and 18 for 11a and 24 and 36 for 16a) as shown in Figure 45(a, b)

For 64-QAM (Data rate 12 and 18 for 11a and 24 and 36 for 16a) as shown in Figure 46(a, b)

2. Conclusion

This work derives the necessary results for the final unified hardware to be implemented in FPGA. Following are the key points to summarize the work done so far.

1) Understanding of PHY layers of 11a and 16a standards is achieved.
2) SIMULINK based simulation provides the reference for the final design.
3) In the SIMULINK system, the mappings of BPSK, QPSK, 16QAM and 64 QAM are achieved at the receiver in presence of Rayleigh multipath fading.
4) For statistical analysis the mechanism of exporting the simulation data to the Excel worksheet is developed.
5) The entire system works according to IEEE 802.11a and 802.16a physical layer specifications as per the choice selected in the system settings blocks. Hence unification is achieved.

The simulation is performed for both 11a and 16a PHY configurations.

References

For a standard citation
1. IEEE Std 802.11a, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, High-Speed Physical Layer in the 5 GHz Band. 2007.
2. IEEE Standard for Local and metropolitan area networks Part 16: Air Interface for Broadband Wireless Access Systems, 2009.

For a book citation
3. J. Terry and J. Heiskala, *OFDM WIRELESS LANs: A Theoretical and Practical Guide*. SAMS, 2001.
4. Matthew Gast, *Wireless Networks,* O'Reilly, 2002.

For a paper citation
5. S. A. Fechtel, OFDM: From the Idea to Implementation, 2005.
6. Choi, S., Philips Research Labs, OPNET Model of the 802.11a Protocol, 15 November, 2000.
7. Prasad, R., van Nee, R., *OFDM for Wireless Multimedia Communications*, Artech House, 2000.
8. Chow, C. C. and Leung, V. C. M., "Performance of IEEE 802.11 Medium Access Control Protocol Over a Wireless Local Area Network with Distributed Radio Bridges,".
9. Alden J. Doyle, K. Han, S. Nadkarni, K. Seshadrinathan, R. Simha, Ian C. Wang, "Performance Evaluation of the IEEE 802.16a PHY Layer Using Simulation", EE381K-11 (14980) wireless communications project report.
10. Carl Eklund, Roger B. Marks, Kenneth L. Stanwood and Stanley Wang, "IEEE Standard 802.16: A Technical Overview of the WirelessMAN Air Interface for Broadband Wireless Access", IEEE Communications Magzine, vol.40, no.6, pp.98-107, June 2002.